

REMARKS

Claims 1-3, 9 and 17 are pending. By this Amendment, claims 1 and 17 are amended. Reconsideration based on the above amendments and the following remarks is respectfully requested.

Applicants appreciate the courtesies shown to Applicants' representative by Examiner Hu in the January 21, 2004 personal interview. Applicants' separate record of the substance of the interview is incorporated into the following remarks.

No new matter is added by this Amendment. Support for the amended language of claims 1 and 17 may be found in the original specification, for example including Figures 1A-1E and page 22, line 22 to page 23, line 4.

I. Rejections Under 35 U.S.C. §103(a)

The Office Action rejected claims 1-3 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,494,835 to Bruel ("Bruel '835") in view of U.S. Patent No. 5,374,564 to Bruel ("Bruel '564") and/or Japanese Patent No. 4-025114 ("JP '114"). The Office Action rejected claim 9 under 35 U.S.C. §103(a) as unpatentable over Bruel '835 in view of Bruel '564 and/or JP '114 and further in view of U.S. Patent No. 6,271,101 to Fukunaga. Claim 17 is rejected under 35 U.S.C. §103(a) as unpatentable over Bruel '835 in view of Bruel '564 and/or Japanese Patent No. 5-313195 ("JP '195"). These rejections are respectfully traversed.

The method of manufacturing a semiconductor substrate according to the present invention has a non-obvious feature, in which said method includes the processes of: forming an insulation film on at least a surface of a semiconductor substrate main body; forming an ion shield member having a predetermined shape on said insulation film; implanting ions into said semiconductor substrate main body from a side on which said insulation film is formed,

to thereby form an ion implantation layer; removing said ion shield member; laminating said insulation film and a support substrate onto each other; and separating said semiconductor substrate main body from said support substrate at a portion of said ion implantation layer, wherein a shape of an outer edge of said ion shield member is tapered, and thereby said ion implantation layer is formed with at least two different depths which are continuous via an inclined portion thereof in response to said tapered shape of the outer edge of said ion shield member.

According to the present invention, a specific construction of the ion implantation layer is obtained owing to using the “tapered” ion shield member. Namely, the ion implantation layer is formed with at least two different depths which are continuous via the inclined portion thereof in response to the tapered shape of the ion shield member. As a result, the incompleteness of the cleavage or separating at the ion implantation line of the single crystal substrate is eliminated, and thereby the yield of the product is improved.

On the other hand, JP '114 relates to a technology of preventing a resist profile from being formed as a so-called trapezoidal shape, in order to obtain a high contrast resist pattern. That is, JP '114 is dedicated to form the resist pattern so that the outer edge thereof becomes precisely or at least 90°. In order to provide a solution for the above-mentioned specific problem, the outer edge of JP '114 must have the essential feature of at least 90°. Thus, in contrast to the present invention, JP '114 is limited to the outer edge having an essential feature of at least 90°.

For the foregoing reasons, Applicants respectfully submit that Bruel '835 in view of Bruel '564 and/or JP '114, alone or in combination, would not have led one of ordinary skill in the art to the invention of claims 1-3. Reconsideration and withdrawal of this rejection are respectfully requested.

With regard to claim 17, JP '195 discloses an active matrix device, in which a part of a silicon layer corresponding to a driver circuit is formed of a CMOS circuit, and a part of the silicon layer corresponding to a switching transistor is formed thinner than the part of the silicon layer corresponding to the driver circuit. In JP '195, in fact, there is description about a "tapered field oxide." This "tapered field oxide" however refers to a so-called "bird's beak," which is inevitably formed as a result of "oxidation of silicon." JP '195 refers to this "bird's beak" merely for the reason that a PMOS transistor is suitable for the switching transistor and a NMOS transistor is not. On the other hand, the "tapered ion shield member" according to the present invention is intentionally formed for the specific purpose, i.e. obtaining the aforementioned specific construction of the ion implantation layer and thereby eliminating the incompleteness of the cleavage (or separating) and consequently improving the yield of the product. Thus, the "tapered" shape according to JP '195 is different from that of the present invention in its origin, function and purpose. Incidentally, as a matter of course, there is no description or suggestion about the cleavage at the ion implantation line, in JP '195.

For the foregoing reasons, Applicants respectfully submit that Bruel '835 in view of Bruel '564 and/or JP '195, alone or in combination, would not have led one of ordinary skill in the art to the invention of claim 17. Reconsideration and withdrawal of this rejection are respectfully requested.

II. CONCLUSION

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-3, 9 and 17 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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